Microprocessor and Computer Architecture

Course Title: Microprocessor and Computer Architecture **Full Marks:** 60+20+20

Course No: BIT153 **Pass Marks:** 24+8+8

Nature of the Course: Theory + Lab **Credit Hrs:** 3

Semester: II

Course Description:

This course provides an in-depth understanding of microprocessors and computer architecture. It covers the internal organization of microprocessors, instruction sets, memory hierarchy, and various components of computer systems. Topics include the study of modern processor architectures, pipelining, cache memory, and input/output mechanisms.

Course Objectives:

By the end of this course, students should be able to:

- Understand the fundamentals of SAP architectures.
- Demonstrate assembly language programming for 8085.
- Describe and evaluate different CPU designs, including pipelined and parallel architectures.
- Analyze memory hierarchies, including caches and virtual memory systems.
- Understand how input/output devices interact with the CPU and memory.

Course Contents

Unit 1: Overview of Microprocessor (4 Hrs)

Components of a Microprocessor: Registers, ALU, Control and Timing, System Buses, Microprocessor Systems with Bus Organization, Introduction to SAP1 and SAP2

Unit 2: 8085 Microprocessor (7 Hrs)

Functional Block Diagram and Pin Configuration, Timing and control Unit, Registers, Data and Address Bus, Intel 8085 Instructions, Operation Code and Operands, Addressing Modes, Interrupts, Flags, Institutions and Data Flow inside 8085, Basic Assembly Language Programming Using 8085 Instruction Sets

Unit 3: Register Transfer Language (4 Hrs)

Microoperation, Register Transfer, Language, Register, Register Transfer, Control, Function, Arithmetic Microoperations, Binary Adder, Binary Adder-Subtractor,

Arithmetic Circuit, Logic Microoperations, Applications of Logic Microoperations, Shift Microoperations, Logical Shift, Circular shift, Arithmetic Shift.

Unit 4: Basis Computer Architecture (7 Hrs.)

Instruction Code, Operation Code, Stored Program Concept, Registers and memory of Basic Computer, Common Bus System for Basic Computer, Instruction Format, Instruction Set Completeness, Control Unit of Basic Computer, Control Timing Signals, Instruction Cycle of Basic computer, Determining Type of Instruction, Memory Reference Instructions, Input-Output Instructions, Program Interrupt & Interrupt Cycle.

Unit 5: Control Unit (3 Hrs.)

Control Word, Microprogram, Control Memory, Control Address Register, Address Sequencing, Conditional Branch, Mapping of Instructions, Subroutines, Microinstruction Format, Symbolic Microinstructions.

Unit 6: Central Processing Unit (4 Hrs.)

Major Components of CPU, CPU Organizations (Single Accumulator Organization, General Register Organization, Stack Organization), Instruction Formats, Addressing Modes, Data Transfer and manipulation, Program Control, Subroutine Call and Return, Types of Interrupt, RISC vs CISC.

Unit 7: Pipelining (5 Hrs.)

Parallel Processing, Multiple Functional Units, Flynn's Classification, Pipelining: Concept and Demonstration with Example, Speedup Equation, Floating Point addition and Subtraction with Pipelining, Instruction Level Pipelining: Instruction Cycle, Three & Four-Segment Instruction Pipeline, Pipeline Conflicts and Solutions, Concept of Vector Processing.

Unit 8: Computer Arithmetic (4 Hrs.)

Addition and Subtraction with Signed Magnitude Data, Addition and Subtraction with Signed 2's Complement Data, Booth Multiplication, Division of Signed magnitude Data, Divide Overflow.

Unit 9: IO Organization (4 Hrs.)

Input-Output Interface: I/O Bus and Interface Modules, I/O vs Memory Bus, Isolated vs Memory-Mapped I/O, Asynchronous Data Transfer: Strobe, Handshaking, Modes Of Transfer: Programmed I/O, Interrupt-Initiated I/O, Direct memory Access, Overview of Priority Interrupt, Input-Output Processor.

Unit 10: Memory Architecture (3 Hrs.)

RAM and ROM Chips, Memory address Map, Memory Connection to CPU, Associative Memory, Read Operation, Write Operation, Cache Memory: Locality of Reference, Hit & Miss Ratio, Mapping (Direct, Associative, Set Associative).

Laboratory Works

The laboratory exercises should be performed using the 8085 trainer kit. The programming tasks should include base conversions, arithmetic operations, conditional branching, and similar concepts.

Recommended Book

- Ramesh S. Gaonkar: Microprocessor Architecture, Programming, and Applications with 8085, prentice Hall
- Morris Mano: Computer system Architecture, Third Edition, prentice Hall
- Computer Architecture: A Quantitative Approach" **by** John L. Hennessy, David A. Patterson.