Rajarshi Janak University
Faculty of Science, Technology and Engineering
Course of Study for B.Sc.CSIT
(First Semester/First Year)

Course Title: Digital Logic
Nature of Course: Theory (3Hrs) +lab (3 Hrs.)
Credit Hrs: 3 Hrs

Course Code: CSIT 105
Full Marks: Ext(40+20)+Int(40)
Pass Marks: Ext(16+8)+Int(16)

Course Description:
This modules is a foundational course that explores the principles and applications of digital systems. Students will learn the fundamentals of Boolean algebra, logic gates, combinational and sequential circuits, and the design of digital systems. Emphasis is placed on developing problem-solving skills through the analysis and synthesis of digital circuits. Practical applications in computing, communication, and embedded systems are also covered to provide real-world context. This course combines theoretical concepts with hands-on laboratory sessions to equip students with the knowledge and skills required for designing and implementing digital systems.

Course Learning Objectives:
By the end of this course, students will be able to:

1. Understand the fundamental principles of digital systems and Boolean algebra.
2. Analyze and design combinational logic circuits using logic gates and minimization techniques.
3. Understand the operation and applications of sequential circuits, including flip-flops, counters, and registers.
4. Develop skills to implement digital circuit designs using hardware description languages (e.g., Verilog) and simulation tools.
5. Apply digital logic concepts to solve real-world problems in computing and electronic systems.
6. Demonstrate proficiency in the use of laboratory equipment and software for the design and testing of digital systems.

Course Contents

Unit 1
Number System and Computer Codes **[7 hrs]**
Introduction, Types of number system, Applications, Weighted Number Systems, Conversions among number Systems, Binary Arithmetic,1's and 2's Complement,9's and 10's complement, Addition and Subtraction of Binary Numbers, Non-Weighted Number Systems: BCD code, Gray code, XS-3 code, Parity, Even and Odd Parity, BCD adder, Error detection and correction technique

Unit-2
Boolean algebra and Logic Gates [**7 hrs]**

Introduction, Signals, Analog and Digital Signals, Boolean Algebra, Truth Tables, Laws and Theorems of Boolean Algebra, Representation of Boolean Functions, Review of Basic Logic gates, Universal Gates, Arithmetic Gates, Implementations using Logic Gates, NAND and NOR Implementations, Positive and Negative Logic

Unit-3

Simplification of Boolean Functions and Combinational Logic [7 hrs]

K-Map, Truth Table to Karnaugh Map Sum-of-Products Method , Pairs, Quads, and Octets, Karnaugh Simplifications, Don't-care Conditions, Product-of-sums Method, conversion of SOP to POS and Vice-versa, Multi-Level NAND and NOR Circuits, Product-of-sums simplifications

Unit-4

Data-Processing Circuits [8 hrs]

Adders: Half Adder, Full Adder, Parallel Binary Adder, Subtractors: Half Subtractor, Full Subtractors, Multiplexers, De-multiplexers, Decoder, BCD to Decimal Decoders, Seven Segment Decoders, Encoders, Exclusive-OR Gates, Parity Generators and Checkers, Code Converter, Magnitude Comparator, Programmable Array Logic(PAL), Programmable Logic Arrays(PLA), Read-Only Memory(ROM)

Unit-5

Sequential Circuits [7 hrs]

RS Flip-Flops, Gated Flip-Flops, Edge-triggered RS FLIP-FLOP, Edge-triggered D FLIP-FLOPs, Edge triggered JK FLIP-FLOPs , FLIP-FLOP Timing, JK Master-slave FLIP-FLOP, Various Representation of FLIP-FLOPs, Conversions of Flip-Flops, Applications of FLIP-FLOPs ,Design using state equation and state reduction table.

Unit 6

Registers, Counters and Memory [5hrs]

Registers: Types of Registers, Serial In - Serial Out, Serial In - Parallel out, Parallel In - Serial Out, Parallel In - Parallel Out, Universal Shift Register, Applications of Shift Registers, **Counters:** Asynchronous Counters, Decoding Gates, Synchronous Counters, Changing the Counter Modulus. Decade Counters, Pre-setable Counters, Counter Design as a Synthesis problem, Basic Memory Operations and Types

Unit-7 [2hrs]

Finite State Machines: Mealy State Machine, Moore State Machine, Components of ASM Charts

Unit-8

Logical Processor Design [3 hrs]

Processor Organization, Arithmetic and Logic Unit, Design of Arithmetic Circuit, Design of Logic Circuit, Design of Arithmetic Logic Unit, Status Register, Design of Shifter

Laboratory Works:

The laboratory work includes implementing the concept of digital electronics using different kit. Also the instructor can use the different online or offline simulation or VHDL software to demonstrate the working of different circuits.

1. Familiarization of logic gates and different kit
2. Combinational circuits
3. Code converters
4. Proof of De-Morgan's Theorem
5. Adder and Subtractors
6. Sequential Circuits
7. Flip-Flops
8. Counters

Text Books/Reference Books

1. Floyd, *"Digital Fundamentals"*, PHI
2. M Morris Mano, *"Digital Logic and Computer Design"*, Pearson, 2017.
3. Stephen Brown, ZvonkoVranesic, *"Fundamentals of Digital Logic Design with VHDL"*, 2nd Edition,Tata McGraw Hill,2005.
4. R D Sudhaker Samuel *"Illustrative Approach to Logic Design"*, Sanguine-Pearson, 2010.